

DIVISIONAL PATENT APPLICATION
of

PAVEL N. LAPTEV
Santa Barbara, California

for

UNITED STATES LETTERS PATENT

on

SYSTEM FOR, AND METHOD OF, ETCHING A SURFACE ON A WAFER

Attorney Docket No.: SPUTT-65056

Sheets of Drawings: Four (4); Figures: (4)

Attorneys

FULWIDER, PATTON, LEE & UTECHT, LLP
Howard Hughes Center
6060 Center Drive, Tenth Floor
Los Angeles, CA 90045

EXPRESS MAIL NO. EV325905283US

BACKGROUND OF A PREFERRED EMBODIMENT OF THE INVENTION

This application is a division of application 09/829,587 (attorney's file SPUTT-56141) filed in the United States Patent and Trademark Office on February 6, 2001.

This invention relates to apparatus for, and methods of, etching a surface of a wafer to provide a fresh and clean surface for providing a deposition on the surface. More particularly, the invention relates to apparatus for, and methods of, etching a surface of an insulating layer in a wafer, and etching walls defining a socket in the wafer, so that the etchings of the surface of the insulating layer, and the etching of the surfaces of the walls in the socket, are smooth and uniform and so that the surfaces do not have any pits.

BACKGROUND OF THE INVENTION

Integrated circuit chips are being used now in all kinds of apparatus to provide complex electrical circuitry for controlling different operations or for providing data and mathematical calculations in business, education, science and many other fields. With
5 successive advances in time, the size of the integrated circuit chips has progressively decreased, particularly because the thickness of the electrical leads in the chips has progressively decreased. Even as the chips have decreased in size, the circuitry on the chips has become progressively complex.

The integrated chips are formed in wafers, each of which holds a number,
10 hundreds and often even thousands, of integrated circuit chips. The chips on the wafer are formed from a plurality of successive layers. Some of the layers provide electrical insulation. Others of the layers are electrically conductive. Electrical pegs or vias are provided between the different electrically conductive layers. The electrical pegs or vias are disposed in sockets provided in insulating layers in the chips. When the fabrication of the wafers has been
15 completed, each chip defines electrical circuitry which performs specialized, often complex, operations.

The fabrication of the different layers in an integrated circuit chip has to be precise. For example, the width and thickness of the circuit leads in the different layers have to be precise in order to maintain the proper impedance values for different components in the
20 circuits. If the proper impedance values are not maintained, the operation of the circuitry in the integrated circuit chip is impaired. Variations in the width and thickness of the circuit leads can result from impurities in the surfaces of different layers in the chips and from uneven and non-smooth surfaces on the insulating layers on which electrically conductive material is

deposited. The criticality in maintaining surfaces even and smooth has increased as the thickness of the leads on the integrated circuit chips has decreased.

Apparatus has existed for a considerable number of years to etch the surfaces of different layers on the chips. The purpose of the etching has been to clean and refresh the surfaces to receive subsequent layers of deposition. The etching has produced uneven surfaces on the layers, thereby producing variations in the characteristics of the electrical material subsequently deposited on the uneven surfaces. The problem has been aggravated as the thickness of the layers has decreased. Attempts have been made to resolve this problem by making the etched surfaces even and uniform. The attempts have provided significant success but improvements in the smoothness and evenness of the surfaces of the insulating layer are constantly desired.

BRIEF DESCRIPTION OF A PREFERRED EMBODIMENT OF THE INVENTION

First and second electrodes at opposite ends and magnets between the electrodes define an enclosure. Inert gas (e.g. argon) molecules pass into the enclosure through an opening near the first electrode and from the enclosure through an opening near the second electrode. A
5 ring near the first electrode, a plate near the second electrode and the magnets are at a reference potential (e.g. ground).

The first electrode is biased at a high negative voltage by a high alternating voltage to produce a high intensity electrical field. The second electrode is biased at a low negative voltage by a low alternating voltage to produce a low intensity electrical field.
10 Electrons movable in a helical path in the enclosure near the first electrode ionize inert gas molecules.

A wafer having a floating potential and having an insulating layer is closely spaced from the second electrode. The electrode and the wafer define plates of a first capacitor having a dielectric formed by inert gas molecules and ions between the plates to provide a high
15 impedance. The wafer and the gas ions in the enclosure define opposite plates of a second capacitor, in series with the first capacitor, having the insulating layer as the dielectric to define a low impedance.

The first capacitor accordingly controls and limits the speed at which the gas ions move to the insulating layer surface to etch this surface. The resultant etch, only of a relatively
20 few angstroms, of the insulating layer is smooth, uniform and accurate even in holes as for vias and does not have any pits.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

Figure 1 is a schematic elevational view of apparatus constituting a preferred embodiment of the invention for etching a surface of an insulating layer in a wafer to produce an even and uniform surface, without any pits on the insulating layer;

Figure 2 is an enlarged fragmentary simplified schematic elevational view of the construction of a wafer, and;

Figure 3 is an enlarged schematic elevational view of electrical fields produced in an enclosure by the apparatus shown in Figure 1, the wafer being disposed in the enclosure;

Figure 4a is an enlarged fragmentary elevational schematic view showing the disposition of particular ones of the components in the preferred embodiment of Figure 1;

Figure 4b is an enlarged fragmentary schematic circuit diagram showing the electrical equivalent of the components in Figure 4a as a pair of capacitors in series, one of the capacitors having a high impedance and the other capacitor having a low impedance;

Figure 5a is an enlarged fragmentary schematic elevational view showing the disposition in the prior art of the particular ones of the components shown in Figure 4a; and

Figure 5b is an enlarged fragmentary schematic circuit diagram showing the electrical equivalent of the disposition of the prior art components in Figure 5a as a single capacitor having a low impedance.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT OF THE INVENTION

Figures 1-4 show a preferred embodiment, generally indicated at 10, of apparatus for etching a surface 12 of an insulating layer 14 in a wafer generally indicated at 16. As will be appreciated, the wafer may be formed from a plurality of stacked layers, some of them electrically conductive and others electrically insulating. In addition to the insulating layer 14, an electrically conductive layer 15 and an electrically insulating base layer 17 are schematically shown to represent the different layers in the integrated circuit chip. The insulating layer 14 may have a plurality of a grooves or sockets 18. The insulating layer 14 may illustratively be made from a suitable material such as a polyamide.

The insulating layer 14 may illustratively have a thickness of approximately three (3) microns. The sockets 18 may be completely, or partially, formed through the thickness of approximately three (3) microns in the insulating layer 14. Figure 2 illustratively shows the sockets 18 as extending completely through the thickness of the insulating layer 14. The preferred apparatus 10 of this invention illustratively may etch approximately one hundred angstroms (100 Å) from the surface 12 of the insulating layers 14 in a smooth and even layer and without any pits in the layer.

The apparatus 10 includes an enclosure 20 which may be formed in part by an electrode 22, an electrode 24 displaced from, but preferably substantially parallel to, the electrode 22 and magnets 26 and 28 disposed in a transverse (preferably substantially perpendicular) relationship to the electrodes 22 and 24. The electrode 22 is disposed in a contiguous and substantially parallel relationship to the wafer 16 and is movable in position toward or away from the wafer, as indicated by a double-headed arrow 25. The spacing between the wafer 16 and the electrode 22 may illustratively be in the order of 0.1 - 2mm. A plate 30 extending from the magnet 26 in a substantially parallel, but spaced, relationship to the electrode

22 also defines the enclosure 20. A ring 32 extending from the magnet 28 to a position spaced from, but contiguous to, the electrode 24 also defines in part the enclosure 20.

The magnets 26 and 28 preferably constitute permanent magnets but they may also constitute magnetizable members on which windings are disposed to produce a saturable magnetic flux when a current flows through the windings. The magnets 26 and 28 may have a north polarization (indicated by the letter "N" in Figure 1) at their positions of contiguity and may have a south polarization (indicated by the letter "S" in Figure 1) at their opposite ends.

The magnets 26 and 28, the plate 30 and the ring 32 are provided with a reference potential such as a ground 34. The wafer 16 is disposed in close proximity to the electrode 22 within the enclosure 20 and in substantially parallel relationship to the electrode. The wafer 16 is at a floating potential.

The electrode 22 receives a relatively low AC voltage from a power supply 36 at a suitable frequency such as approximately 13.56 MHz. As will be explained in detail subsequently, this causes the electrode 22 to receive a relatively low negative DC bias such as a negative bias in the order of -100 volts to -500 volts. A matching network 38 is preferably disposed electrically between the power supply 36 and the electrode 22 to match the impedance of the power supply to the impedance of the electrode.

The electrode 24 receives a relatively high AC voltage from a power supply 40 at a suitable frequency such as approximately 13.56 MHz. As will be explained in detail subsequently, this causes the electrode 24 to have a relatively high negative DC bias such as a negative bias in the order of -1000 volts to -3000 volts. A matching network and zero bias circuit 42 are preferably disposed electrically between the power supply 40 and the electrode 24 to match the impedance of the power supply to the impedance of the electrode and to provide

substantially a ground potential on the electrode. The zero bias circuit may constitute an inductance between the electrode 24 and ground to provide a high impedance for alternating voltages and to provide a low impedance for a DC voltage. The power supplies 36 and 40 may constitute a single power supply.

5 A conduit 44 is provided for introducing molecules of an inert gas such as argon into the enclosure 20 from a source 45. The argon molecules pass into the enclosure 30 through the space between the electrode 24 and the ring 32. The argon molecules pass out of the enclosure 30 through the space between the plate 34 and the wafer 16. The argon gas flow through the enclosure 30 may illustratively be at a flow rate of 0.1-50 SCCM at a working pressure of
10 0.5-5mTorr. The movement of the argon molecules through the enclosure 20 is facilitated by a vacuum pump 47.

 A negative bias is produced on the electrode 22 because of the alternating voltage applied to the electrode. In the positive half cycles of the alternating voltage, the electrode 22 attracts electrons because of the electrical field between the electrode and the ground potential 34
15 on the plate 30. In the negative half cycles of the alternating voltage, positive ions are attracted to the electrode because of the electrical field between the electrode and the ground potential 34 on the plate 30. Since the electrons are considerably lighter in weight than the positive ions, they move faster toward the electrode 22 than the positive ions. This causes the electrons to accumulate in the space adjacent the electrode 22, thereby producing the negative DC bias on the
20 electrode. The electrode 24 receives a negative bias because of the same physical phenomenon. However, the negative bias on the electrode 22 is considerably less than the negative DC bias on the electrode 24 because of the differences in the voltages applied to the electrodes.

As previously indicated, the magnetic field produced by the magnets 26 and 28 is substantially perpendicular to the electrical fields produced by the electrodes 22 and 24. This causes electrons in the enclosure 20 to move in a spiral or helical path between the electrode 22 and the plate 30, and between the electrode 24 and the ring 32, because of the ground potentials on the plate and the ring. The electrons strike molecules of argon gas and ionize these molecules. Since the electrical field between the electrode 24 and the ring 32 is considerably stronger than the electrical field between the electrode 22 and the plate 30, most of the ionization of argon molecules occurs in the region of the electrode 24. Some of these argon ions then move into the region of the electrode 22.

Figure 3 illustrates at 46 lines of force produced by the electrical field between the electrode 22 and the plate 30. Arrows indicate the direction of the lines 46 of force. The electrons in the enclosure 20 travel in a spiral or helical path along the force lines 46, the spiral or helical path resulting from the force of the magnetic field as the electrons move along the force lines 46. In like manner, Figure 3 illustrates at 48 lines of force produced by the electrical field between the electrode 24 and the ring 32 and between the electrode and the grounded magnets 26 and 28. The electrons in the enclosure 20 travel in a spiral or helical path along the force lines 48 because of the force on the electrons by the magnets 26 and 28.

Applicant's assignee of record in this application has previously sold one (1) unit of apparatus with features similar to the apparatus shown in Figure 1. This unit may have been sold more than one (1) year prior to the date of this application. However, there is one significant difference between the apparatus 10 constituting the preferred embodiment of the invention and the unit previously sold by applicant's assignee. The significant difference is that the wafer 16 engaged the electrode 22 in the one (1) unit sold prior to the date of this application.

The circuit equivalent of this arrangement is shown in Figure 5b and is indicated as prior art in that Figure. As previously indicated, the wafer 16 is separated from the electrode 22 in the preferred embodiment 10 of this invention.

As will be seen, the combination of the electrode 22 and the wafer 16 in Figure 5a is seen as a single electrode or plate in a capacitor 50 in Figure 5b. The other electrode or plate in the capacitor 50 is defined by the positive ions in the enclosure 20 at positions adjacent the electrode 24. These positive ions are schematically illustrated by dots (.) at 51 in Figure 3. The dielectric between the plates of the capacitor 50 may be considered to be the insulating layer 14. The impedance of the capacitor 50 is accordingly relatively low because the insulating layer 14 is relatively thin and because the dielectric constant of the insulating layer is lower than the dielectric constant of air or the dielectric constant of a vacuum.

Since the impedance of the capacitor 50 is relatively low, a relatively large current flows through the capacitor. This current results from the attraction of the argon ions to the insulating layer 14 because of the negative DC voltage on the electrode 22. The relatively large current produces an etching of molecules and ions from the surface 12 of the insulating layer 14. This etching is of such a force that the etching is not smooth, even or uniform. Pitting of the surface of the insulating layer 14 accordingly occurs. The problem is particularly aggravated in considering the etching of the walls of the sockets 18 in the insulating layer 14.

Since the etching does not result in a smooth, even and uniform surface 12 of the insulating layer 14, any subsequent deposition of an electrically conductive layer on the surface 12 has significant differences in thickness of the electrically conductive material at different positions on the surface 12. This significantly affects the electrical characteristics of the

electrical deposition on the insulating layer 14 and produces significant deterioration in the performance characteristics of the integrated circuit chips formed from the wafer.

As previously indicated, the wafer 16 is separated from the electrode 22 in the preferred embodiment 10 of this invention. The separation may be in the order of 0.1 to 2.0 millimeters. This causes two (2) capacitors 52 and 54 in Figure 4b to be defined by the electrode 22, the wafer 16 and the charge produced by the argon ions 51 in the enclosure 20 in the vicinity of the electrode 22. The plates of the capacitor 52 in Figure 4b may be respectively considered to be defined by the electrode 22 and by the electrically conductive deposition layers in the wafer 16. Although there may be argon ions in this gap, the argon ions are relatively small in number. Furthermore, the gap is so small that the argon ions cannot be accelerated to any significant degree. Because of these factors, the dielectric in the capacitor 52 in Figure 4b may be considered to be the gap between the electrode 22 and the wafer 16. This gap causes the impedance of the capacitor 52 to be relatively high. This impedance can be adjusted to any desired value by adjusting the position of the electrode 22 in the opposite directions 25 to vary the distance between the electrode and the wafer 16.

The capacitors 52 and 54 may be considered to be in series as shown in Figure 4b. The capacitor 54 may be considered to have plates defined by the electrically conductive layers in the wafer 16 and by the charge provided by the argon ions 51 in the enclosure 20 in the vicinity of the electrode 20. The dielectric for the capacitor 54 may be considered to be the insulating layer 14. The impedance of the capacitor 54 is relatively low, particularly in relation to the impedance of the capacitor 52, because of the thin dimension of the insulating layer 14 and the dielectric constant of the insulating layer.

The current through the series circuit including the capacitors 52 and 54 in Figure 4b is limited and controlled by the capacitor 52 because of the high impedance of the capacitor. This limited and controlled current provides a gentle etching of the surface 12 of the insulating layer 14 and of the walls of the sockets 18. As a result, any specified amount of material may be etched from the surface 12 of the insulating layer 14 and from the walls of the sockets 18. For example, an etching of the material of the insulating layers 14 and the walls of the sockets 18 may be provided in a thickness of approximately one hundred angstroms (100 Å).

The etching produces smooth, even and uniform surfaces of the insulating layer 14 by the apparatus 10 as a result of the etching. This provides for a deposition of a smooth, uniform and even thickness of an electrically conductive material on the etched surface of the insulating layer 14. The etching of the walls in the sockets 18 is also even, uniform and smooth. This constitutes a distinct advance over the prior art, even the prior art as represented by the single unit of the apparatus sold by applicant's assignee prior to the filing date of this application, this prior unit being shown in Figure 5a and being represented by the electrical circuitry shown in Figure 5b.

As shown schematically in Figure 4a, balls 60 made from a suitable material such as copper may be provided on the electrically conductive surface of the wafer 160. The balls 60 operate as electrical leads. The balls 60 are known in wafers of the prior art. The balls 60 are not affected by the actions of the capacitances 52 and 54 in Figure 4b.

Although the invention has been disclosed and illustrated with relation to particular embodiments, the principles involved are capable of being used in numerous other embodiments which will be apparent to persons of ordinary skill in the art. The invention is, therefore, to be limited only as indicated by the scope of the appended claims.